

5 light and accumulating the charge for a predetermined
6 period of time;
7 a vertical transfer unit for vertically transferring
8 charge from the pixels in the pixel unit, a horizontal
9 transfer unit for horizontally transferring charge from the
10 vertical transfer unit;
11 shift gates each provided between each pixel and the
12 vertical transfer unit for reading out the charge in the
13 pixels to the vertical transfer unit, gate electrodes for
14 controlling the shift gates; and
15 a plurality of lead lines and a plurality of
16 connection terminals for connecting the gate electrodes to
17 an external circuit,
18 gate control lines connected to gate electrode groups
19 in which horizontal lines belonging to each coset of modulo
20 N within successive pixel rows are connected commonly, N
21 being a predetermined natural number between 4 and one half
22 the number of pixels in a column, and also being a minimum
23 number corresponding to a periodic unit of gate electrode
24 connections to said connection terminals within said
25 successive pixel rows, being combined with each other so as
26 to reduce the number of the connection terminals to less
27 than N .

Please replace claim 3 with the following:

1 3. (TWICE AMENDED) A solid-state imaging device
2 comprising:
3 a pixel unit constituted by a two-dimensional array of
4 pixels for generating charge in correspondence to received
5 light and accumulating the charge for a predetermined
6 period of time;

7 a vertical transfer unit for vertically transferring
8 charge from the pixels in the pixel unit, a horizontal
9 transfer unit for horizontally transferring charge from the
10 vertical transfer unit;

11 shift gates each provided between each pixel and the
12 vertical transfer unit for reading out the charge in the
13 pixels to the vertical transfer unit, gate electrodes for
14 controlling the shift gates; and

15 a plurality of lead lines and a plurality of
16 connection terminals for connecting the gate electrodes to
17 an external circuit,

18 the gate electrodes being provided in a predetermined
19 number N of gate electrode groups such that horizontal line
20 number of the gate electrode groups which are connected to
21 respective common lead lines belong to each same residue
22 class of modulo N, N being a predetermined natural number
23 between 4 and one half the number of pixels in a column,
24 and also being a minimum number corresponding to the
25 periodic unit about connections to said connection
26 terminals within said successive pixel rows, some of the
27 gate electrode groups being commonly connected so that the
28 connection terminals are less in number than N.

cl
cont
Please replace claim 4 with the following:

1 4. (TWICE AMENDED) A solid-state imaging device
2 comprising:

3 a pixel unit constituted by a two-dimensional array of
4 pixels for generating charge in correspondence to received
5 light and accumulating the charge for a predetermined
6 period of time;

7 a vertical transfer unit for vertically transferring
8 charge from the pixels in the pixel unit, a horizontal
9 transfer unit for horizontally transferring charge from the
10 vertical transfer unit;

11 shift gates each provided between each pixel and the
12 vertical transfer unit for reading out the charge in the
13 pixels to the vertical transfer unit, gate electrodes for
14 controlling the shift gates;

15 and a plurality of lead lines and a plurality of
16 connection terminals for connecting the gate electrodes to
17 an external circuit,

18 the gate electrodes making up N of gate electrode
19 groups in which the lines belonging to each coset of modulo
20 N within successive pixel rows are connected to common lead
21 lines, N being a predetermined natural number between 4 and
22 one half the number of pixels in a column, and also being a
23 minimum number corresponding to a periodic unit of gate
24 electrode connections to said connection terminals within
25 said successive pixel rows, the gate electrode groups
26 having common connections to reduce the number of the
27 connection terminals to less than N,

28 wherein the commonly connected gate electrode groups
29 are always controlled in the same way in each of all
30 predetermined read-out modes including selective pixel
31 read-out modes by selective shift gate driving.

Please replace claim 5 with the following:

1 5. (TWICE AMENDED) A solid-state imaging device
2 comprising:

3 a pixel unit constituted by a two-dimensional array of
4 pixels for generating charge in correspondence to received
5 light and accumulating the charge for a predetermined
6 period of time;

7 a vertical transfer unit for vertically transferring
8 charge from the pixels in the pixel unit, a horizontal
9 transfer unit for horizontally transferring charge from the
10 vertical transfer unit;

11 shift gates each provided between each pixel and the
12 vertical transfer unit for reading out the charge in the
13 pixels to the vertical transfer unit, gate electrodes for
14 controlling the shift gates; and

15 a plurality of lead lines and a plurality of
16 connection terminals for connecting the gate electrodes to
17 an external circuit,

18 gate control lines connected to gate electrode groups
19 in which the horizontal lines belonging to each coset of
20 modulo N within successive pixel rows are connected
21 commonly, N being a predetermined natural number between 4
22 and one half the number of pixels in a column, and also
23 being a minimum number corresponding to a periodic unit of
24 gate electrode connections to said connection terminals
25 within said successive pixel rows, being combined with each
26 other so as to reduce the number of the connection
27 terminals to less than N ,

28 wherein the commonly connected gate electrode groups
29 are always controlled in the same way in each of all
30 predetermined read-out modes including selective pixel
31 read-out modes by selective shift gate driving.

Please replace claim 6 with the following:

1 6. (TWICE AMENDED) A solid-state imaging device
2 comprising:
3 a pixel unit constituted by a two-dimensional array of
4 pixels for generating charge in correspondence to received
5 light and accumulating the charge for a predetermined
6 period of time;
7 a vertical transfer unit for vertically transferring
8 charge from the pixels in the pixel unit, a horizontal
9 transfer unit for horizontally transferring charge from the
10 vertical transfer unit;
11 shift gates each provided between each pixel and the
12 vertical transfer unit for reading out the charge in the
13 pixels to the vertical transfer unit, gate electrodes for
14 controlling the shift gates; and
15 a plurality of lead lines and a plurality of
16 connection terminals for connecting the gate electrodes to
17 an external circuit,
18 the gate electrodes being provided in a predetermined
19 number N of gate electrode groups such that horizontal line
20 number of the gate electrode groups which are connected to
21 respective common lead lines belong to each same residue
22 class of modulo N, N being a predetermined natural number
23 between 4 and one half the number of pixels in a column,
24 and also being a minimum number corresponding to the
25 periodic unit about connections to said connection
26 terminals within successive pixel rows, some of the gate
27 electrode groups being commonly connected so that the
28 connection terminals are less in number than N,
29 wherein the commonly connected gate electrode groups
30 are always controlled in the same way in each of all
31 predetermined read-out modes including selective pixel
32 read-out modes by selective shift gate driving.

Please cancel claim 10 without prejudice to, or disclaimer of, the subject matter recited therein.

Please add the following new claim:

525
D1

--11. (NEW) A solid-state imaging device comprising:

- a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;
- a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit;
- shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, and a plurality of R gate electrodes for controlling the shift gates; and
- a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

cancel

- wherein the R gate electrodes are divided into S gate groups, each gate group having R/S gate electrodes,
- wherein the R gate electrodes are divided into R/S pixel groups, each having R/(R/S) consecutive, adjacent, gate electrodes,
- wherein the i^{th} gate electrode of each pixel group, where $i = 1$ to $R/(R/S)$, share a common connection terminal, and
- wherein at least two gate electrodes within a given pixel group share a common connection terminal.--

In accordance with 37 C.F.R. § 1.121(c)(1)(ii), separate sheets with the rewritten claims marked-up to show